Narrow VDC Extended Battery Life (EBL) Technique

Presentation

September 2003

Overview

- Present Situation: Large voltage range of supply voltage (V_{DC}) to system voltage regulators (VRs)
  - VR design can be improved with narrower V_{DC} range
- Proposed Solution: Narrow VDC EBL Technique
  - Reduce the voltage range of V_{DC} using a system charger VR
  - VRs can be optimized because of narrower voltage range
    - Increase efficiency and reduce board area
  - Power path switch and battery path switch can be removed
    - Reduces power loss and board area

Narrow VDC

- **Option #1:** Using existing battery pack
  - Compatible with existing battery packs
  - Uses system charger VR
  - Removes power path switch
  - Lower power consumption and saves PCB area

- **Option #2:** Using a modified battery pack
  - Uses system charger VR and modified battery packs
  - Removes power path switch and battery charger switch
  - Even lower power consumption and saves more PCB area than Option #1

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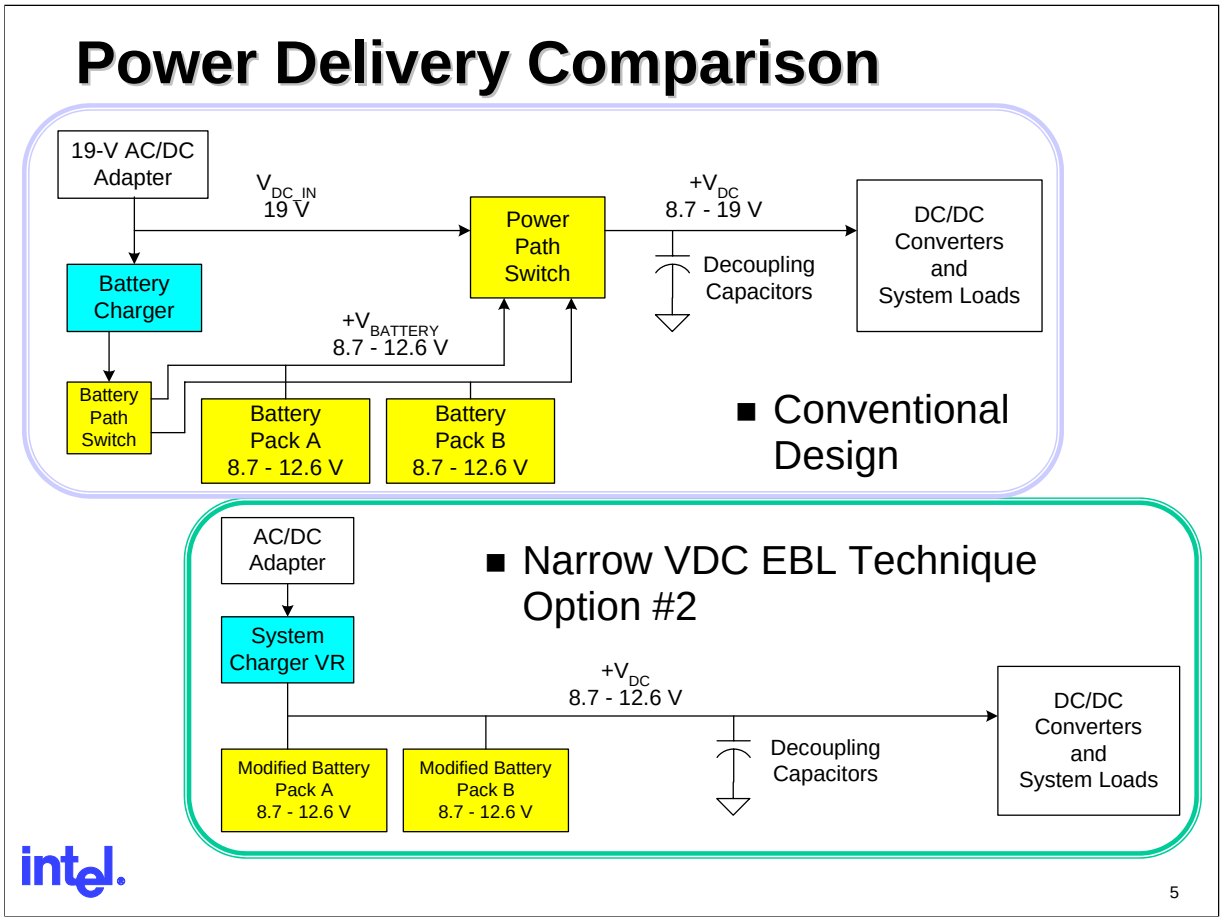
The objective of Narrow VDC EBL Technique is to reduce power loss by reducing the voltage range of the V_{DC} node. The V_{DC} node is the input power from which all other power rails are derived.

The voltage range reduction is accomplished by replacing the battery charger circuit with a system charger VR (implemented by modifying the battery charger circuit). The change from battery charger to system charger VR narrows the V_{DC} range (enabling DC/DC converter optimizations in the system) and allows the removal of the power path switch, saving additional power and board area. This technique is called Narrow VDC EBL Technique Option #1.

Narrow VDC EBL Technique Option #2 modifies the battery packs as well. In addition to the benefits of Option #1, the battery charger switch can also be removed.

The following pages describe Option #2 in detail and is followed by the description of Option #1.



The top drawing is a block diagram of a conventional two-battery power delivery solution for today's laptop designs. V_{DC} comes from the batteries (through the power path switch) or directly from the AC/DC adapter. The adapter sets the upper bound of the V_{DC} range (in this example 19 V) and the minimum battery voltage is the lower bound of the V_{DC} range. In this example, the batteries are assumed to be in a 3-series stack configuration of Li-Ion cells. This means the voltage supplied from the batteries will range from 8.7 to 12.6 V. Therefore, the V_{DC} voltage in a conventional design can range from 8.7 to 19 V. The DC/DC converters from which all the power rails are derived need to be designed to operate efficiently across the entire range.

By reducing the input voltage range, these system voltage regulators can be optimized to save power and area.

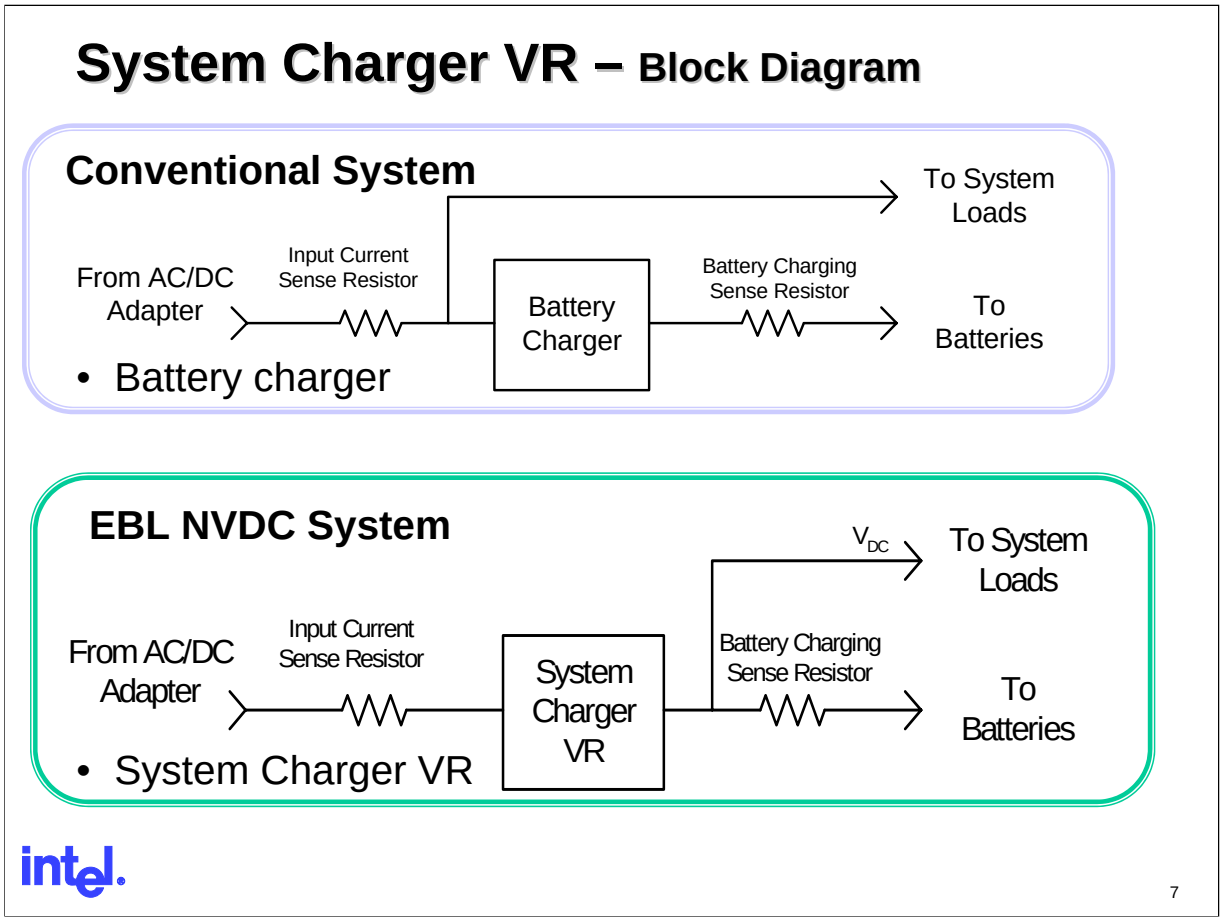
The bottom diagram shows the changes that occur when implementing Narrow VDC EBL Technique Option #2. The Battery Charger is modified to function as a System Charger VR and the V_{DC} is supplied off the regulated output of the System Charger VR. The battery packs are modified to allow the system to select them directly, removing the need for the battery path switch. The power path switch is also removed and this simplification of the power delivery solution saves power and board area.

System Charger VR Overview

- Objectives
  - Provide narrower voltage range to input of system DC/DC converters
  - Functions as a battery charger
- Implementation
  - Re-design battery charging circuit as system charger VR circuit
- Benefits
  - Lower V_{DC} maximum voltage
    - Enables reduced power dissipation and area
  - Application circuits available from some vendors
  - Intel is working with many vendors to produce optimized SCVR controllers

Changing the battery charger into a system charger VR is what enables the reduction of the upper bound of the V_{DC} voltage. This circuit can typically be constructed from a battery charger with specific application circuitry or circuitry designed for this function. At the time of this writing, there is already a released product that can be used as a system charger VR without additional circuitry beyond what is typically used for a battery charger.

The following pages examine the system charger VR in more detail.

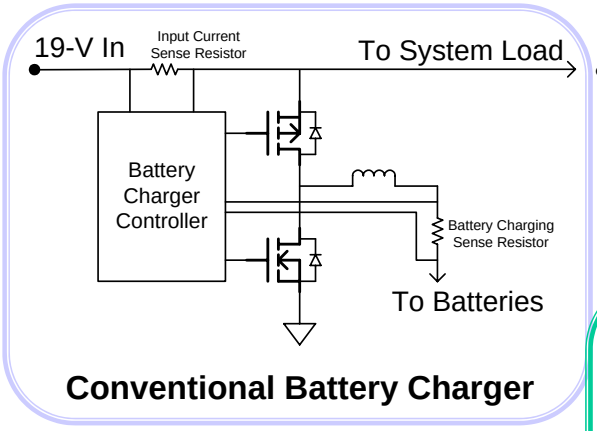


In the top figure, an example of a simplified conventional power path is shown. The power from the AC/DC adapter flows through a input current sense resistor and to the battery charging circuit and the system loads. The line to the system loads is “unregulated” because it comes directly from the AC/DC adapter. There is also a battery charging sense resistor that senses the current drawn to charge the batteries and is used to monitor battery charging.

The input current sense resistor is used to monitor the current being supplied by the adapter and enables reducing the power supplied to charge the batteries during times of large system load demand.

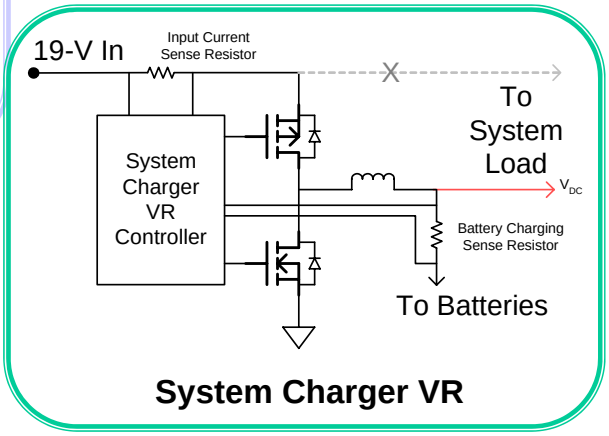
In the Narrow VDC System, a system charger VR is used instead of the battery charging circuit and the system load is pulled from the “regulated” output of the system charger. In this way, the Narrow VDC system is quite similar to the conventional system with battery charger.

System Charger VR – Schematics



Conventional Battery Charger

- Output of battery charger only charges batteries



System Charger VR

- Charger output sensing must be modified

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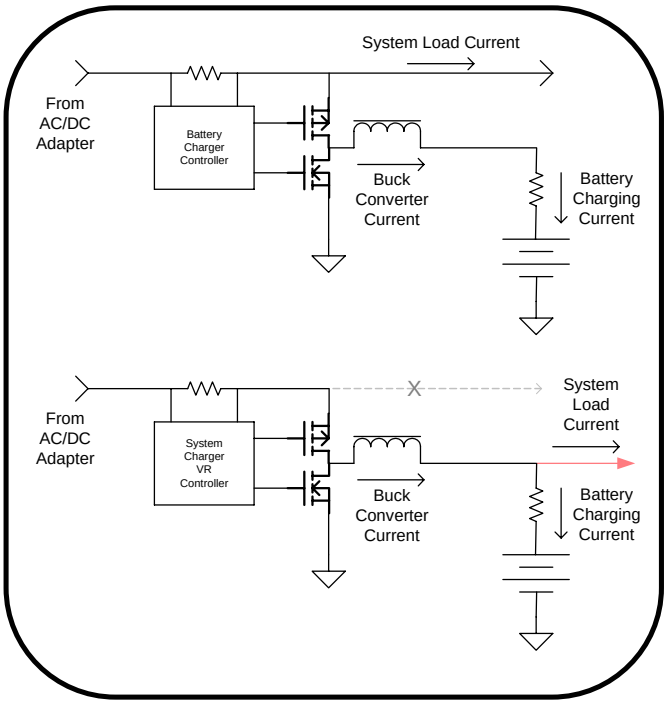
A conventional battery charger is essentially a step-down (buck) converter that supplies the appropriate voltage and current to the batteries. The system load is connected to the unregulated input to the buck converter. The batteries are connected to the regulated output of the buck converter.

In a Narrow VDC implementation, the battery charger controller is replaced with a *system charger VR controller* and this circuit is called a *system charger VR*. The system load as well as the battery charge current comes from the regulated output of the buck converter.

System Charger VR – Buck Converter Current



- Example A
  - Pload max = 25 W
  - Vmax = 8.4 V
  - Vmin = 5.8 V
  - Iload max = ~ 4.3 A
  - Ichg max = ~ 4 A
    - Maximum buck converter current is similar whether system charger VR or battery charger
- Example B
  - Pload max = 70 W
  - Vmax = 12.6 V
  - Vmin = 8.7 V
  - Iload max = ~8 A
  - Ichg max = ~ 5 A
    - Maximum buck converter current is ~ 60% greater when system charger VR compared to battery charger

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When moving from a battery charger to a system charger VR, consideration for the size of FETs and inductor needs to be taken into account because of the potential of increasing the load on the buck converter. Presented here are two examples:

Example A is based on the Intel Concept PC called Newport that was demonstrated at IDF Spring 2003. This system is a ULV processor-based convertible tablet design and used a 2-series battery configuration. The peak electrical system load is 25 W. Because the battery is a 2-series stack, the minimum V_{DC} voltage is 5.8 V. That means the maximum system load is approximately 4.3 A. The battery pack in this system is charged at a 4 A current. Thus, the buck converter load current requirements are similar for charging the batteries and powering the system load. In order to control the cost of the AC/DC adapter and buck converter, the battery charging current is reduced as the system load current increases.

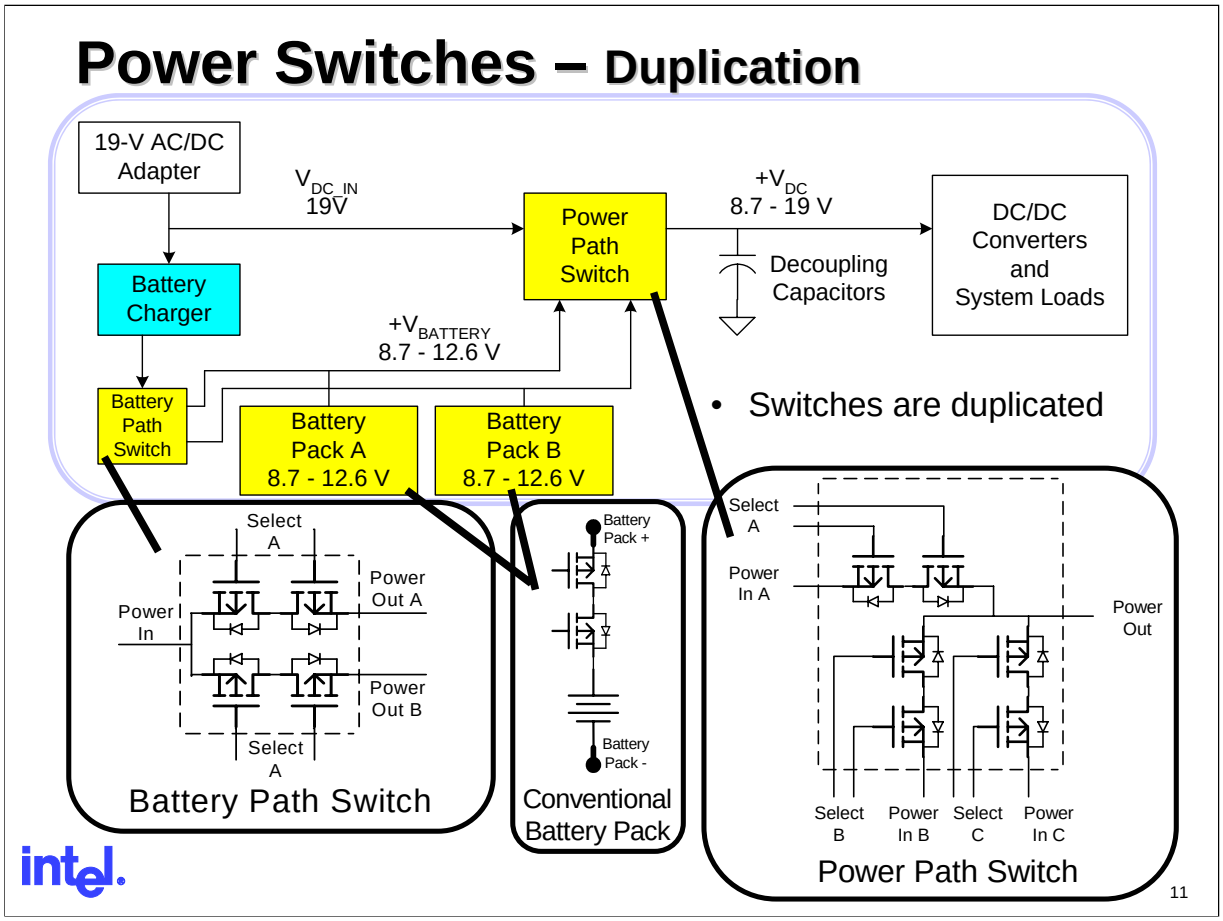
Example B is a hypothetical 70-W peak system load design with a 3-series stack battery. In this configuration, the maximum system current is approximately 8 A. The battery charger would have been designed to handle around 5 A of current. The system charger VR will now have to handle 60% more current that the battery charger, so components will most likely need to be upgraded. Adding two more FETs and using a larger inductor will handle the higher current and incurs a cost increase.

Also, note that when the batteries supply the system load, all current travels upward through the battery charging sense resistor. An extra FET will need to be placed across this FET and turned on when running off batteries to reduce power dissipation in the power delivery path.

Modified Battery Pack Overview

- Objective: Incorporate battery selection circuit in battery packs
- Implementation
  - Design systems to incorporate modified battery packs
  - Use modified battery packs
- Benefits
  - Elimination of redundant components
  - Reduced power dissipation and area

In order to fully utilize the advantages of implementing the Narrow VDC EBL Technique, the batteries should be modified. Through the modification of the battery pack, some redundant FETs in the power path are removed, saving power, money, and area as shown in the following pages.



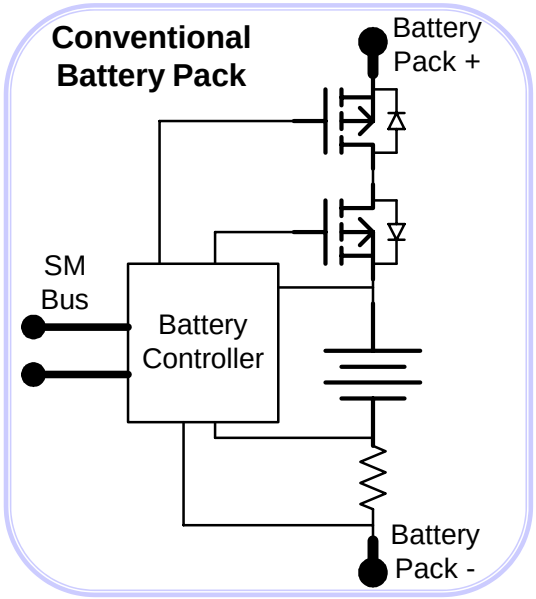
In this figure, typical circuit diagrams for the battery path switch, the battery pack, and the power path switch are shown.

In the case where the batteries are being charged, current is flowing through both the battery path switch and the two FETs in the battery pack. When the batteries are supplying power to the system, current flows through the battery FETs and through two of the FETs in the power path switch. Each of the FETs shown must handle similar currents and are similar to each other. They are also redundant since all current must flow through the battery pack FETs.

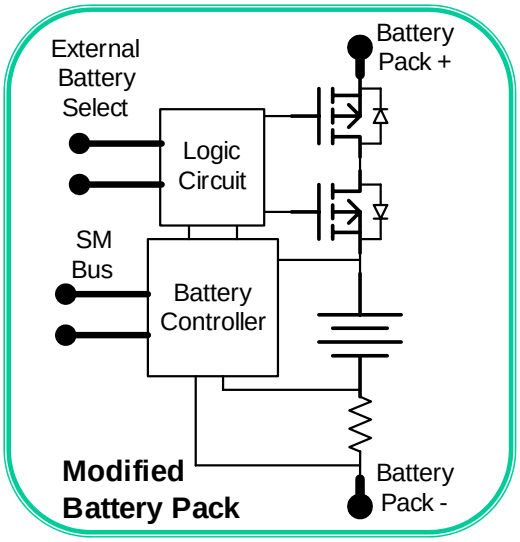
If the battery pack FETs could be controlled (turned off when the battery is not in use) by the system, then the extra FETs in the battery path switch and power path switch could be removed. The system needs the ability to turn off individual batteries because without the battery charger switch or the power path switch in place, the batteries would be shorted together.

Upcoming slides describe how this is accomplished.

Battery Packs – Block Diagram



- Selector control logic added in modified battery pack
  - Additional contacts required on battery pack

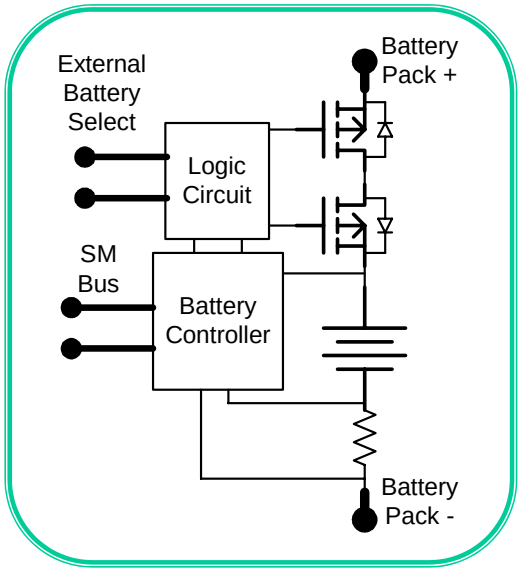


The battery packs need a small amount of logic for the system to gain the ability to turn off the battery when not in use. The addition of two contacts to the battery pack is also necessary for the system to interface with the modified battery pack.

In the future, the small amount of logic can be integrated into the battery controller chip.

Battery Packs – Battery Select

- De-selected by default
  - To avoid shorting batteries when plugging a second battery into a system
- Enabled by low signal
  - Allows system activation when plugging battery into a ‘dead’ system
- 3.3 volt control signals
  - Independent of battery voltage



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As in present systems, the battery controller chip needs to be able to turn off the battery pack when it deems necessary (overcharge, undercharge, and other unfavorable situations). In addition, three new criteria are introduced in a modified battery pack.

First, the battery should be deselected by default.This is to avoid the case where plugging a second battery in a machine connects the two batteries together.

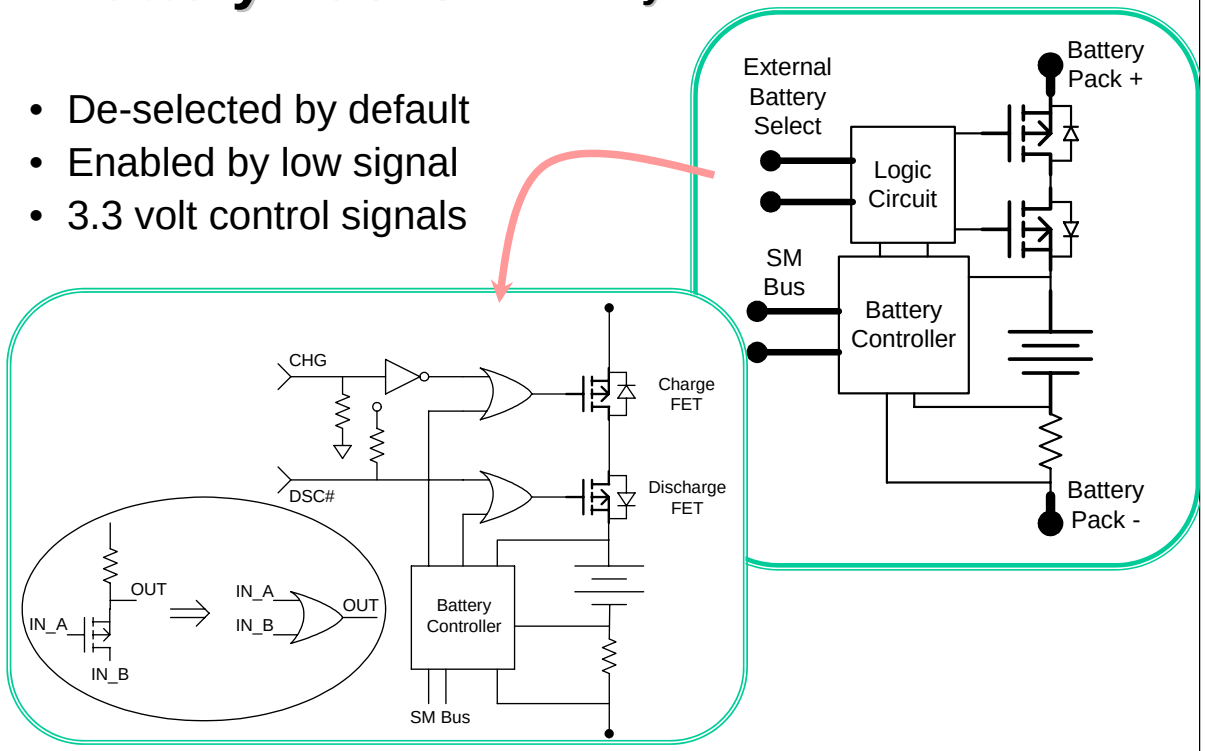
Second, the battery should be enabled by a low signal. In the scenario where a battery is plugged into a system with no power, the only signal the system can provide is a low signal (ground). This requirement allows a battery to be enabled when plugged into a “dead” system.

Third, 3.3-V control signals were specified for the Intel Concept PC. This was a choice made because 3.3 V was readily available and familiar. There is no requirement that the logic run on any particular voltage; any other interface voltage would also be a reasonable choice.

The required logic circuit can be easily implemented as shown in the following slide.

Battery Packs – Battery Select

- De-selected by default
- Enabled by low signal
- 3.3 volt control signals



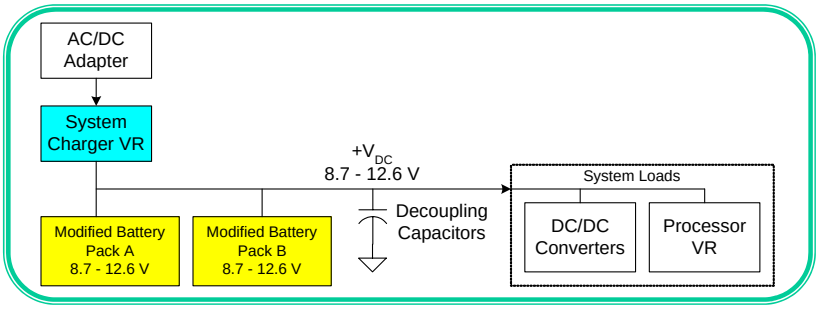
The box on the left contains a detailed view of the diagram on the right, expanding the logic circuit box into a logical schematic.

The OR gates can be implemented, as shown in the bubble, with a resistor and a FET (or two FETs). The inverter can also be implemented as a resistor and a FET or two FETs.

The pull up and pull down resistors on CHG and DSC# fulfill the requirements that the battery be deselected by default and enabled by a low signal.

Not shown here is the level shifting needed for 3.3-V control signals.

Narrow VDC Power Delivery – Savings



	Conventional Processor VR Costs	NVDC Processor VR Costs	NVDC Processor VR Savings	Battery Path Switch and Power Path Switch Costs	Total NVDC Savings
Inductor	2 x 0.8 uH	2 x 0.8 uH			
Cbulk	5 x 330 uF	4 x 330 uF			
Cmlcc	35 x 10 uF	35 x 10 uF			
Cinput	14 x 10 uF @ 25 V	14 x 10 uF @ 16 V			
High Side FET	2 x IRF6604	2 x IRF6604		9 x 20 mohm SO-8 P-FET	
Low Side FET	2 x IRF6607	2 x IRF6607			
Area	796 mm^2	771 mm^2	25 mm^2	252 mm^2	277 mm^2

Source: Intel Corporation (Estimated)

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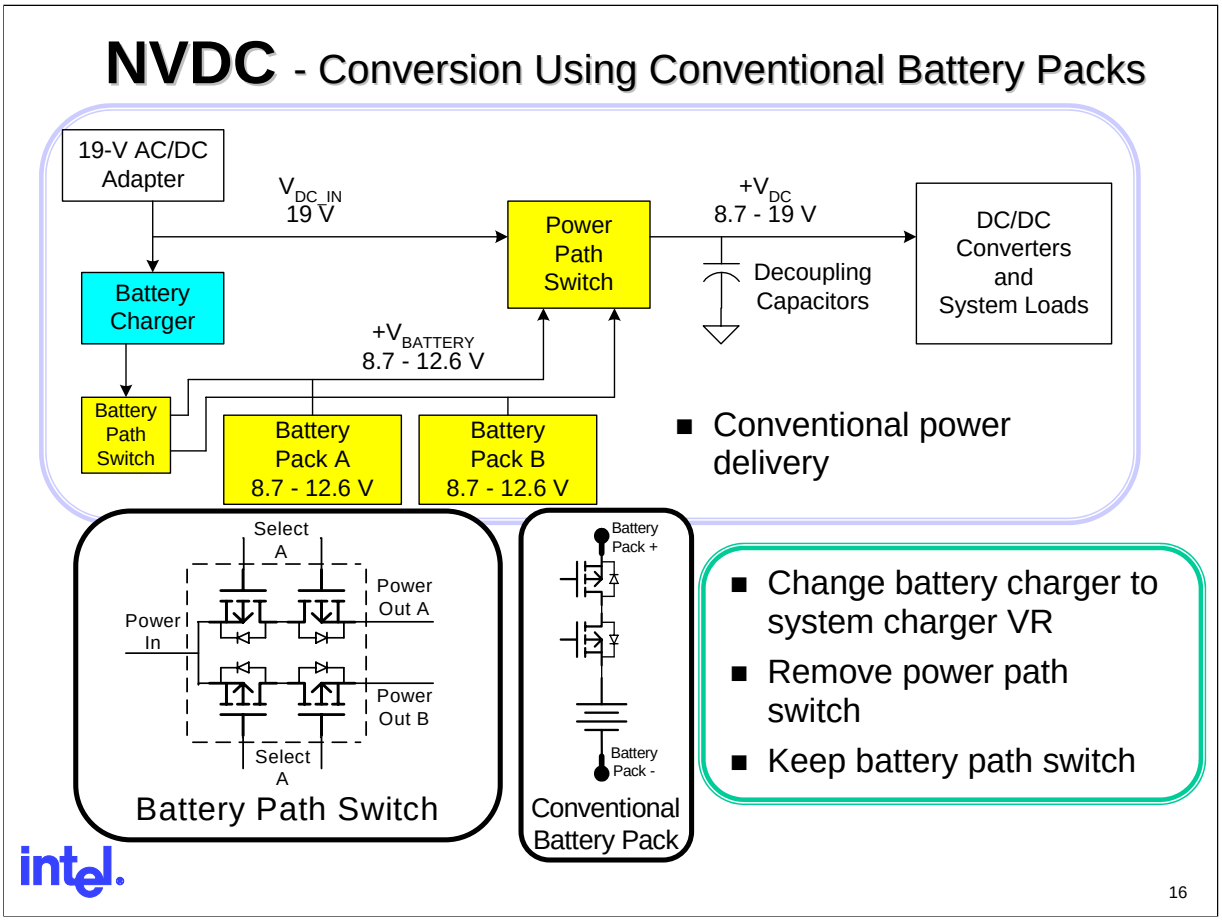
With the replacement of the battery charger with the system charger VR and the replacement of the conventional battery packs with the modified battery packs, the battery path switch and power path switch can be removed. The V_{DC} voltage range is narrowed to 8.7 – 12.6 V. This narrowing of the V_{DC} range allows optimizations to be made in the DC/DC converters.

By implementing Narrow VDC EBL Technique, smaller input capacitors can be used and the number of bulk capacitors used by the processor VR can be reduced. This yields a potential board area savings of approximately 25 mm^2. Note, this is the savings from only the processor VR. Other savings could be gained by doing the same analysis and similar changes to the other DC/DC converters.

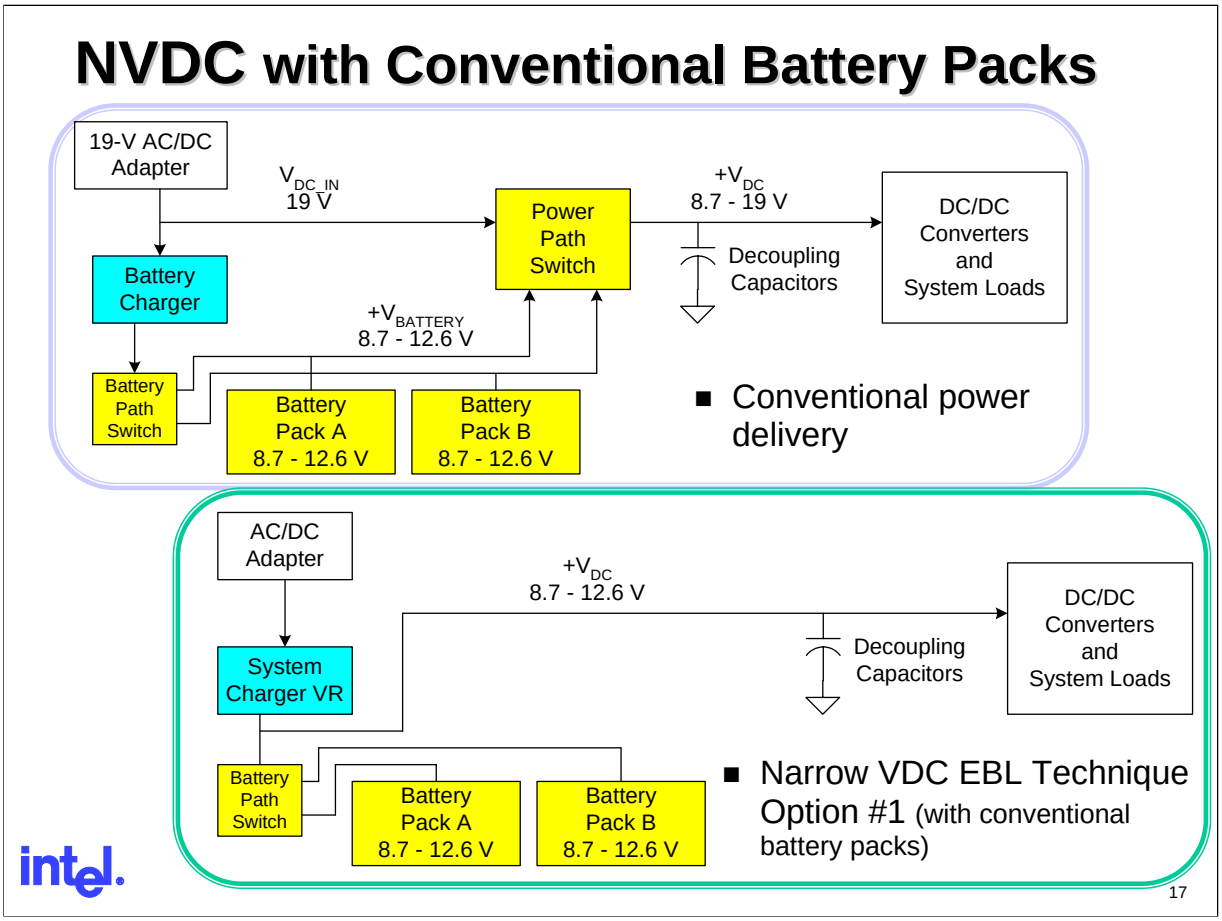
Based on the design shown on page 11, the removal of the battery path switch and the power path switch allowed us to save an additional 10 power FETs. In the system charger VR, it was noted that the addition of a single FET was needed across the battery charging sense resistor, so a total nine FETs is saved. This potentially yields another 250 mm^2.

Power savings are achieved by designing optimized DC/DC converters and avoiding power dissipation in the power path switch FETs.



If battery packs are not modified, one can still implement the Narrow VDC EBL Technique Option #1.

In Option #1, the battery charger is changed to a system charger VR and the power path switch is removed, but the battery path switch is kept in place to control the battery packs.



In this configuration, FETs are saved by eliminating the power path switch and the benefits mentioned before in the optimized DC/DC converters are still gained.